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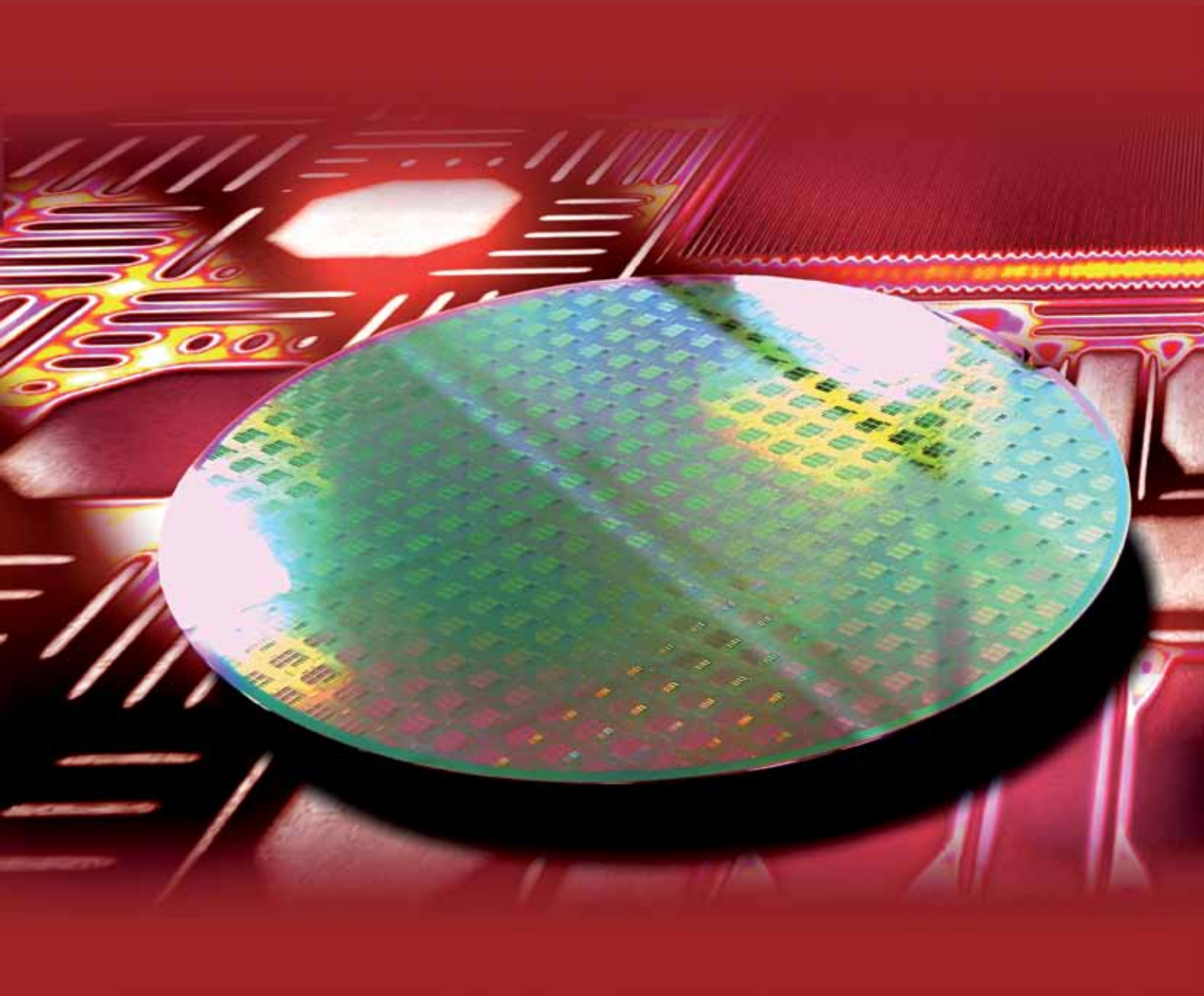
FRAUNHOFER INSTITUTE FOR ELECTRONIC NANO SYSTEMS ENAS

BACK-END OF LINE



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The actual developments of micro and nano technologies are fascinating. Undoubted they are playing a key role in today's product development and technical progress. With a large variety of different devices, different technologies and materials they enable the integration of mechanical, electrical, optical, chemical, biological, and other functions into one system on minimum space.

The Fraunhofer Institute for Electronic Nano Systems ENAS in Chemnitz focuses on research and development in the fields of Smart Systems Integration by using micro and nano technologies with partners in Germany, Europe and worldwide. Based on prospective industrial needs, Fraunhofer ENAS provides services in:

- Development, design and test of MEMS and NEMS (micro and nano electro mechanical systems),
- Wafer level packaging of MEMS and NEMS,
- Metallization und interconnect systems for micro and nano electronics as well as 3D integration,
- New sensor and system concepts with innovative material systems,
- Integration of printed functionalities into systems,
- Reliability and security of micro and nano systems.

Solutions for the Semiconductor Industry

Within Fraunhofer ENAS, the department Back-End of Line focuses on

- Materials and process development,
- Process integration,
- Modeling and simulation

for interconnect systems in ultralarge-scale integrated CMOS devices (ULSI) as well as NEMS components.

In ULSI semiconductor manufacturing, the Back-End of Line technologies comprise all processing steps from the contact level up to the completely processed wafer prior to electrical testing – in other words, the entire interconnect system, including device passivation. Ongoing downscaling has led to numerous diversifications of materials and processes over the past decade, depending largely on the product concerned.

With reduced geometric dimensions of the transistors, the resistance-capacitance product (RC product) of the interconnect system increases, resulting in strongly increasing signal delay. To date, this is one of the main issues faced by the semiconductor industry to further boost the performance of ULSI microprocessors and other logic devices.

Suitable materials, advanced processing methods and analytical tools as well as novel modeling and simulation approaches are required to master these challenges. In this respect, already the past decade was characterized by the introduction of copper technology and low-k dielectrics. Further innovations and challenges are expected in the years to come, for example resulting from the deployment of ultralow-k dielectrics, carbon nanotubes and new processes such as atomic layer deposition (ALD) for ultrathin films.

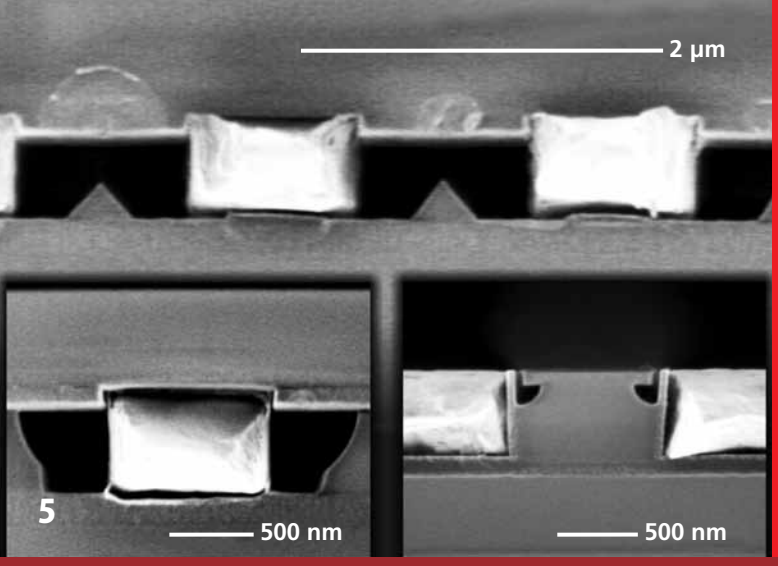
Strong Ties to Chemnitz University of Technology and the Fraunhofer-Gesellschaft

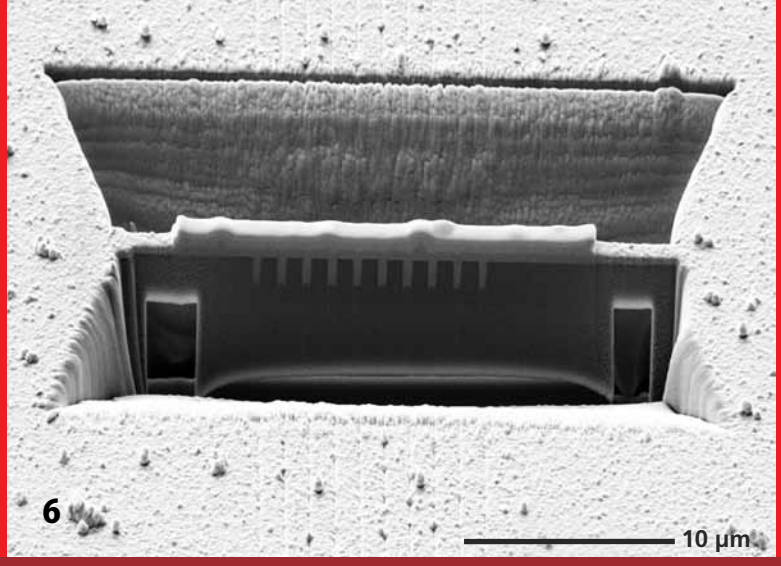
The department closely collaborates with the Center for Microtechnologies (ZfM) at Chemnitz University of Technology. This is not only expressed by shared cleanroom facilities and equipment. Many results of the basic research work carried out at the ZfM have been successfully transferred to application by the Back-End of Line Department at Fraunhofer ENAS. For example, the integration of low-k materials and the development of novel processes such as for the ALD of metals and growth of carbon nanotubes continue to be important areas of work at both institutions.

Developing such new technologies requires new or optimized processes and equipment. More and more often, the experimental work must be backed by theoretical studies and simulations. Therefore, Fraunhofer ENAS together with the ZfM is developing advanced models and simulation tools for processes such as PVD, CVD and CMP, as well as devices.

Apart from the fruitful cooperation with Chemnitz University of Technology, the department Back-End of Line closely collaborates with other institutes of the Fraunhofer Group for Microelectronics and the Fraunhofer Nanotechnology Alliance.

Fig. 1: Wafer inspection at a 200 mm wet bench
Fig. 2: Applied Materials 200 mm cluster system
Fig. 3: Wafer processing on an IPEC CMP equipment
Fig. 4: Thin film characterization by spectroscopic ellipsometry





Processes and Materials

For various applications and business segments including semiconductor and solar cell production, processes are developed, optimized, and provided on a routine basis. In addition, research and development is carried out focusing on the introduction of new materials into standard processing schemes. Focusing mainly on interconnects for on-chip application and 3D integration, the following processes and technologies are available:

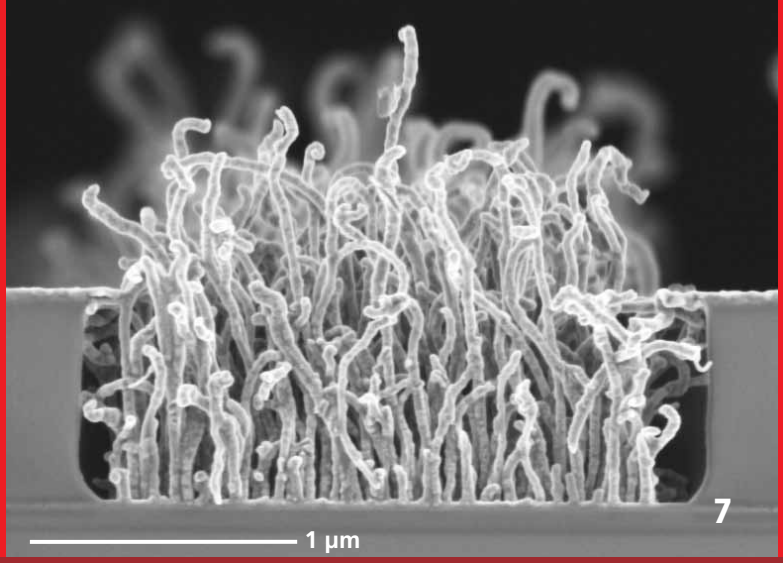
- Barrier and metal chemical vapor deposition (CVD), especially TiN and Cu MOCVD,
- Thermal and plasma-enhanced CVD of dielectrics, such as SiO_2, Si_3N_4, SiC, and SiCOH,
- Atomic layer deposition (ALD) of metals, metal oxides, and nitrides,
- Electrochemical deposition (ECD) of Cu, Ni, Au, and Sn,
- Electroless deposition (ELD) of Ni and Au,
- Growth of carbon nanotubes (CNTs) by CVD and deposition from dispersion by dielectrophoresis,
- Dry etching of metals and dielectrics,
- Wet cleaning and k-restore of ultralow-k (ULK) materials,
- Chemical mechanical planarization (CMP) of Si, SiO_2, and barrier/copper film systems as well as Al, Ge, and various glasses,
- Grinding processes for silicon, glass, lithium niobate, lithium tantalate, and other ceramic substrates,
- Mechanical, electrical, and thermal characterization of low-k and ultralow-k dielectrics.

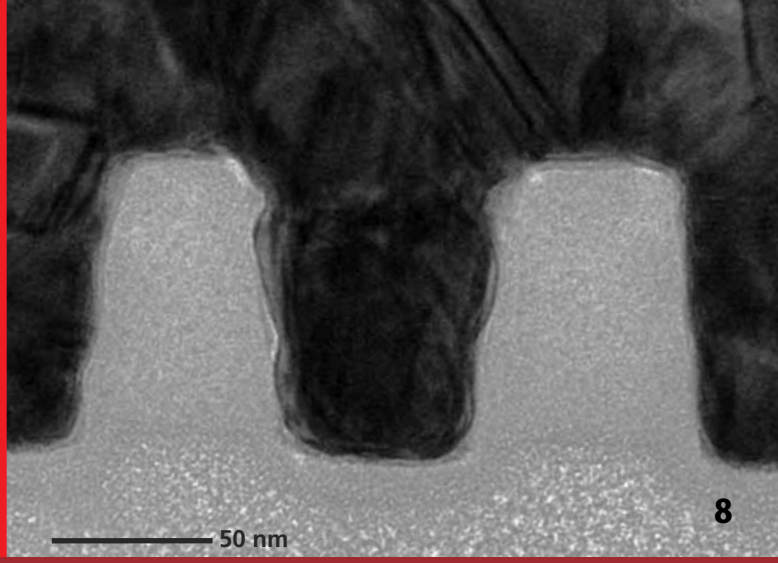
Interconnects for Micro and Nano Electronics

The department Back-End of Line delivers solutions for materials and processes, as well as their integration into interconnect systems for micro- and nanoelectronics.

An **AIRGAP TECHNOLOGY**, developed as the ultimate low-k solution together with the ZfM, is a typical example of this work. The technology is continuously optimized for distinct chip layouts of the upcoming technology nodes. Simulation and characterization results suggest an excellently balanced electrical, thermal, and mechanical behavior.

COPPER DAMASCENE METALLIZATION is an important research area for interconnects in micro- and nanoelectronics. For copper-based metallization schemes, effective diffusion barrier layers are required. Work is therefore directed towards the integation of ultrathin barrier films deposited by PVD, CVD, and ALD. To date, copper deposition for IC metallization relies on electroplating (ECD) on sputtered copper seed layers. Our activities are therefore aiming at optimized ECD processes on ultrathin seed layers. Especially for seed layer growth, atomic layer deposition (ALD) is a field of strong interest at the department Back-End of Line. Research is carried out related to ALD precursor development and screening as well as process development and characterization. As an alternative to ECD copper growth, as well as for applications in 3D integration, the metal-organic chemical vapor deposition (MOCVD) of copper is applied and further optimized to the specific tech-





nological requirements. Especially for multi-level interconnect systems, chemical mechanical planarization (CMP) processes are required. Industry-style equipment is available for process integration and for research purposes, such as screening and evaluation of novel polishing chemicals.

For the **INTEGRATION OF LOW-K AND ULTRALOW-K DIELECTRICS**, cleaning methods for the 45 and 32 nm technology nodes and below are developed. Furthermore, processes for the restoration of the k-value after patterning low-k materials are under investigation. Plasma-based patterning techniques for low-k materials are studied by a variety of in-situ methods such as Langmuir probe, optical emission spectroscopy (OES), and laser absorption spectroscopy. The goal of this work is the optimization of the dry etching processes as well as correlating the etching results with the characterization techniques during the process for an immediate process control.

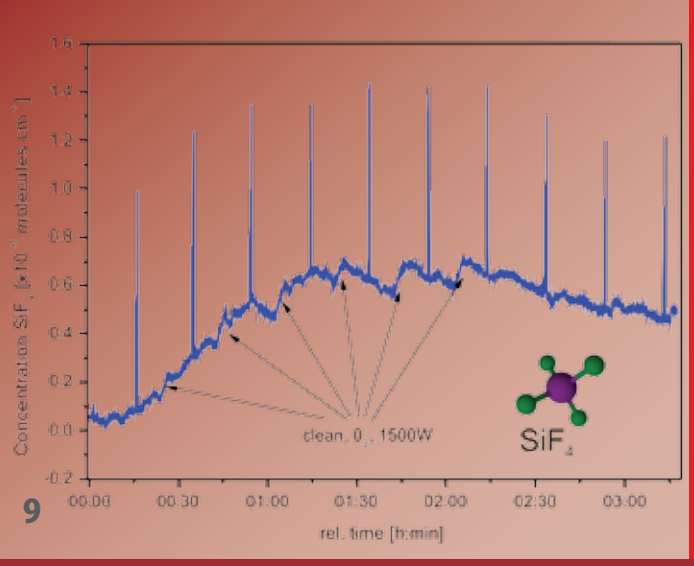
As a radical alternative to metal-based interconnects in future device generations, **CARBON NANOTUBES** (CNTs) are studied. Due to their unique properties, they appear promising for both contacts and vias. In our department, multi-walled CNTs are grown on mono- and bimetallic catalysts with the CVD method. Current work concentrates on integration technologies and low-temperature growth to meet the requirements for application in advanced interconnect systems.

Materials and Metallization for NEMS

Based on the long-term experience in interconnect technology, materials, interconnects, and integration **TECHNOLOGIES FOR NANO-ELECTROMECHANICAL SYSTEMS** (NEMS) are emerging topics at the department Back-End of Line. Due to the unique sensing properties, CNTs appear of particular interest for NEMS-based sensors. Current work concentrates on wafer-level integration and contact formation between metal electrodes and CNTs. In this respect, methods such as dielectrophoresis for the controlled lateral deposition of carbon nanotubes as well as atomic layer deposition (ALD) for functionalization and metallization of CNTs are studied.

Furthermore, **SPINTRONIC MATERIALS** having strong temperature limitations, such as Fe_xCo_y or Cu/Co multilayers for Giant Magneto-Resistance (GMR) sensors, are to be integrated with interconnect process technology. The work includes the development of ALD growth and etching processes for such materials, as well as complete sensor integration.

Fig. 5: Airgap formation between copper interconnects
Fig. 6: FIB-cut TEM lamella of copper interconnects with ALD seed layer
Fig. 7: Selectively grown CNTs coated by ALD
Fig. 8: Nanoscale interconnects homogeneously filled with a TiN barrier and copper by MOCVD



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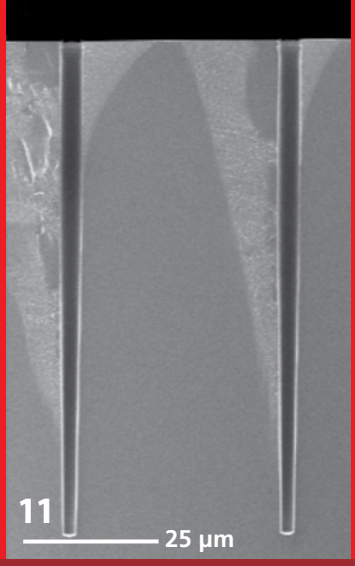

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Technologies for 3D Integration in MEMS Applications

3D integration is of major interest for several applications in the fields of microelectronics and MEMS technology. Hereby, wafers or chips are stacked and interconnected, for example by using Through Silicon Vias (TSVs), to minimize electrical path lengths and thus enhance the electrical and thermal performance as well as to minimize the chip size. 3D integration also provides the opportunity to integrate electronic devices of different functions and technologies, e.g. MEMS devices and the corresponding control and signal processing electronics. Fabrication technologies for 3D comprise methods such as

- TSV formation,
- Wafer thinning,
- Alignment and bonding.

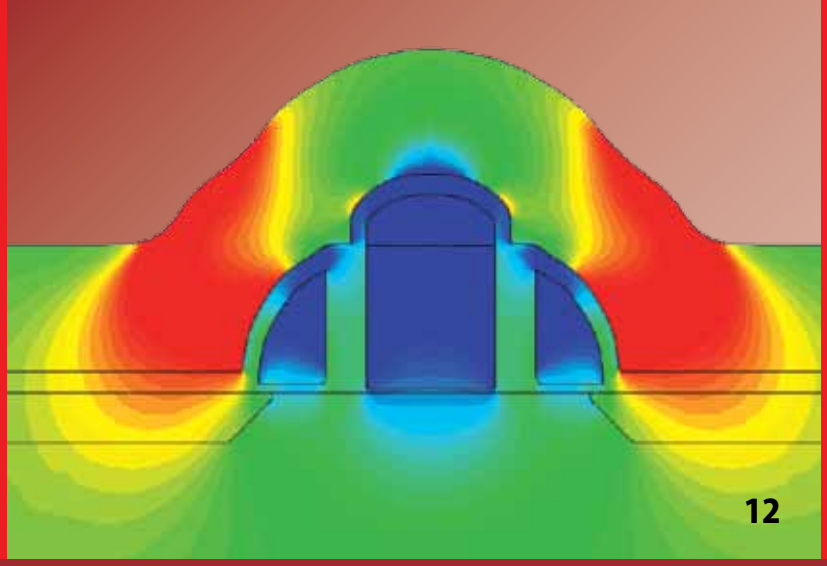
Our experience in the field of 3D integration especially relates to the **TSV FORMATION** for MEMS and sensor applications. For this application field, the higher aspect ratios and larger dimensions compared to TSVs in purely electronic devices are challenging for etching and metallization. Work is therefore directed towards the optimization of different TSV geometries with regard to etching and filling processes and the technological approaches "Via First" and "Via Last". Combining the MOCVD of diffusion barrier and copper films as a special metallization scheme, a highly conformal seed layer can be produced for subsequent filling by ECD. For TSVs smaller than 5 µm, even a complete filling by CVD is possible. To pursue complete technological approaches compliant with different MEMS and sensor requirements, we are closely collaborating with the department Systems Packaging at Fraunhofer ENAS. Industry-scale equipment is available at all stages of the integration process. For the full process chain, we are closely collaborating with Fraunhofer EMFT in Munich, Fraunhofer IZM in Berlin and Fraunhofer IZM-ASSID in Dresden.

Simulation of Devices, Processes, and Equipment

Apart from the experimental research areas, the department Back-End of Line has many years of experience in simulation and modeling of processes and equipment for the semiconductor industry.

As the development of new technologies requires new or optimized processes and equipment, advanced models and simulation tools are specifically designed for PVD, CVD, ALD as well as CMP. They support the development of improved deposition and polishing techniques by optimization of process conditions, tool configuration, and feature topography.

The **SIMULATION OF PVD PROCESSES** has been extensively applied to study the formation of ultrathin metal layers as diffusion barriers for adjoining copper interconnects, as contact layers, or as seed layers for subsequent deposition steps. PVD simulations are able to cover all important aspects of the deposition such as rate, conformity, composition, or energy deposition even for the demanding conditions within small vias or trenches.



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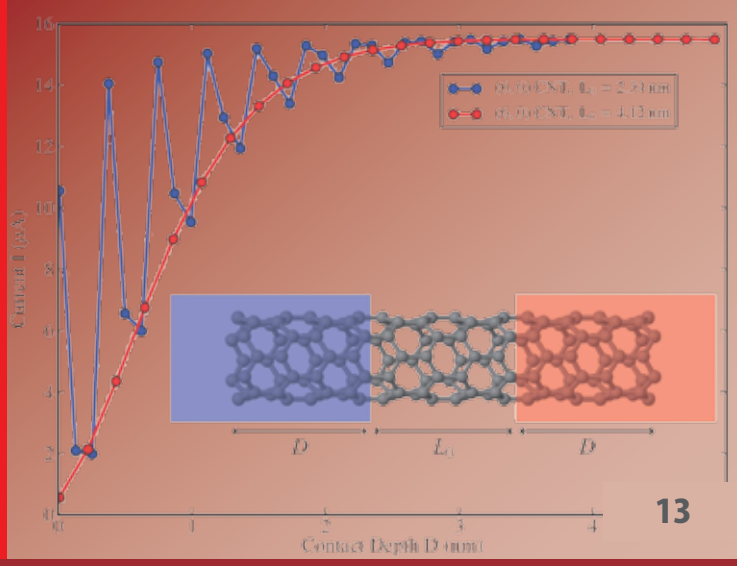

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CVD SIMULATION applies hydrodynamic methods at the reactor scale and ballistic methods at the feature scale. In addition to optimum deposition rates, the uniformity of film thickness and doping across large wafers and batch sizes, as well as conformal film deposition in deep trenches and vias are predicted and optimized.

An emerging field is the **DEVICE SIMULATION** which becomes more and more important for understanding device behavior and optimizing device performance. Using adequate models, the increase of transistor performance induced by stressor films prior to metallization can be predicted. Device simulations are also applied to model the electrical as well as the heat transport within nanoscale interconnects. Besides microelectronics applications, device simulations are also applied to study the influence of novel solar cell concepts on cell efficiency.

SIMULATION AND MODELING OF THE ELECTRICAL RELIABILITY is another key issue on the way to a comprehensive description of the interconnect system. Biased temperature stress (BTS) data from inter-metal dielectrics can be analyzed and compared with various available models in order to investigate the electrical failure mechanisms.

For future nanoelectronic and NEMS devices, modeling of materials properties at the nanoscale is becoming more and more important. Therefore, a new research area is the **AB-INITIO SIMULATION AND MODELING** of transport properties of nanostructures, such as nanoscale Cu interconnects and carbon nanotubes. Furthermore, quantum chemical modeling and simulation supports the development of metal ALD processes.

Analytics

To support the experimental work, the department Back-End of Line has a number of advanced analytical methods at its disposal, such as:

- 200 mm SEM and SEM/FIB tools with state-of-the-art EDX analytics,
- AFM and surface profilometry,
- Spectroscopic ellipsometry,
- FTIR spectroscopy in transmission and reflection mode including ATR,
- Contact angle measurements,
- In-situ methods for monitoring deposition and etching processes,
- Electrical characterization methods.

Fig. 9: SiF_4 concentration during ICP etching detected in situ by quantum cascade laser absorption spectroscopy
Fig. 10: TSV filled with copper by electrochemical deposition
Fig. 11: Optimized etching profile for TSVs with an aspect ratio of 20
Fig. 12: Simulated stress fields within a MOSFET transistor caused by deposition of a nitride stressor film
Fig. 13: Simulation of the role of the contact depth on the electrical current through a CNT-copper contact

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Front page:
200 mm wafer with patterned low-k dielectric for copper damascene metallization

Photos:
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