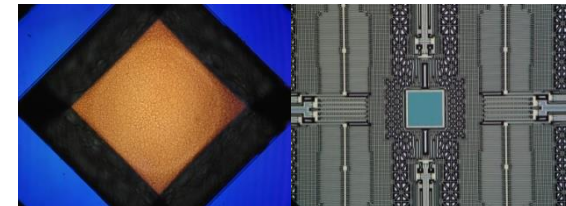
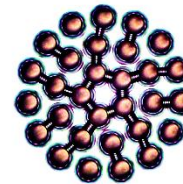
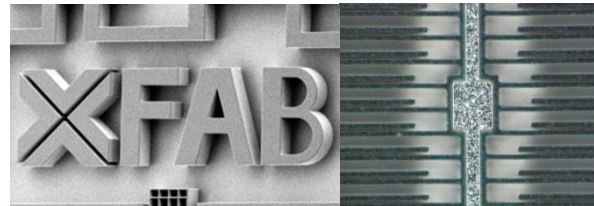


# From sampling to ramping:

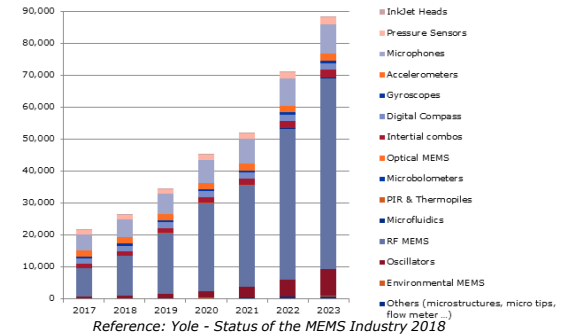
## Technology and Business Model Challenges for a MEMS Foundry to Address WLP Applications



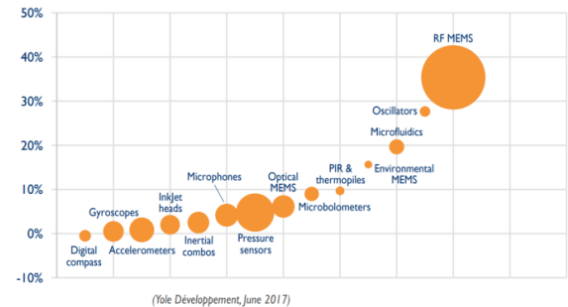
# Kontext



- Yole 2017 “The MEMS and Sensor market is growing and new applications are arriving. However, MEMS companies and MEMS foundries are struggling to grow”
- “Everything looks good - so where is the problem”
- Voice from trenches: “MEMS high volume manufacturing is super complex”



2017-2022 MEMS CAGR for the different MEMS devices  
(bubble sizes are proportional to 2022 market size in M\$)



# About X-FAB



 **Corbeil-Essonnes**

- CMOS, SOI, RF
- Wafer size: 200mm
- Capacity: 35k 200mm equiv. WSPM
- Capacity upside in 9k sqm unused fab space

- CMOS, SOI, MEMS
- Wafer size: 150mm, partly 200mm (MEMS)
- Capacity: 12k 200mm equiv. WSPM



 **Erfurt**



 **Lubbock**

- CMOS, SiC
- Wafer size: 150mm
- Capacity: 15k 200mm equiv. WSPM



 **Itzehoe**

- MEMS
- Wafer size: 200mm
- Wide portfolio of materials, technologies & capabilities



 **Dresden**

- CMOS
- Wafer size: 200mm
- Capacity: 8k 200mm WSPM
- Capacity upside up to 10k WSPM



 **Sarawak**

- CMOS, SOI
- Wafer size: 200mm
- Capacity: 24k WSPM
- Capacity upside above 30k WSPM

**Legend:**

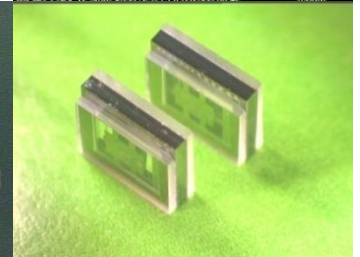
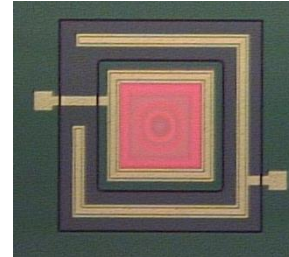
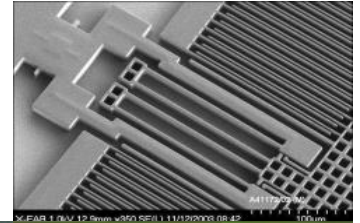
WSPM = Wafer Starts Per Month

## Overview

- High-volume MEMS production operation embedded in CMOS environment
- 200 mm & 150 mm MEMS operations in 4 clean rooms
- Wide range of processes and materials – CMOS and non-CMOS compatible
- MEMS & CMOS integration
- Automotive quality system

## Application examples

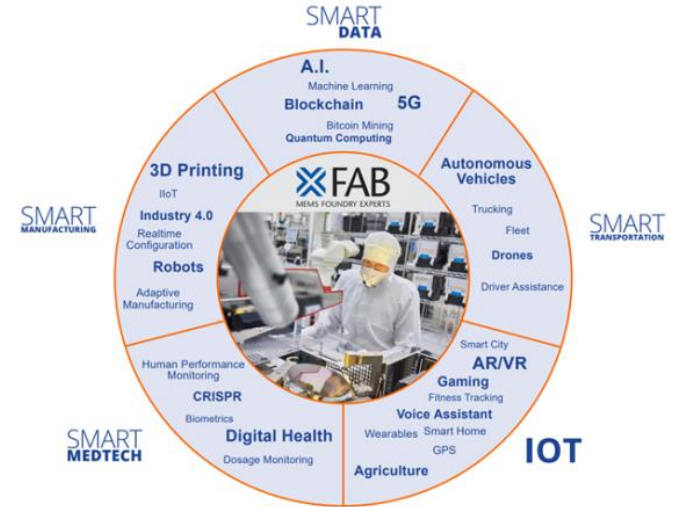
- Automotive
  - Pressure sensors, Inertial sensors
- Medical /  $\mu$ Fludic
  - DNA sequencing, Drug & allergy screening
- Mobile Communication
  - Microphones
- Industrial
  - Gas Sensor



# Business Profile



- 90% of MEMS projects at X-FAB are addressing customer specific technology solutions
  - Typically 3-5 RFQ's per month from all regions
  - 30+ ongoing development programs
  - Concurrent dev't of process and product
  - 30%+ of all programs don't succeed in getting to SOP
- 10% of new MEMS projects are using X-FAB MEMS open platform technologies
  - Readily qualified technologies,
  - DR, Specs, PDKs
  - Pressure Sensor
  - Inertial Sensor

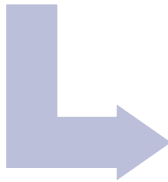


# MEMS Foundry Challenge



Fragmented and diverse  
MEMS market

- One Product
- One Process
- One Package
- One Calibration



Small CUSP Business  
cases

- Opportunity risks
- Large CAPEX
- Utilizing existing tools at and beyond the tool limits
- Concurrent design and technology development
- Diverse technologies
- Long learning cycles

strategic vectors for  
X-FAB

- Business
- Customer
- Technology
- Tools
- Experience
- Methodology

## › Foundry vs. customer selection

- Business case
  - Markets and applications fit
  - Volume, GM, CAPEX
  - Regional fit
  - Experience, expectations, time to market, sampling requirements, NRE
  - Customer relationships

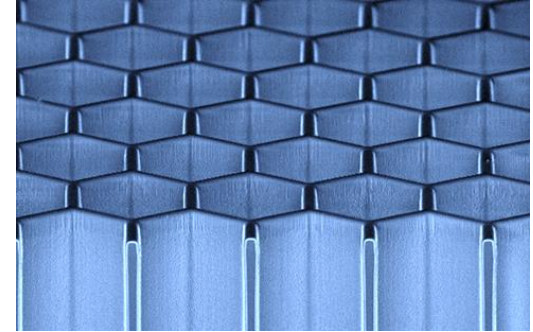
## › Engineering resources

- Development in mfg. environment vs. development in research lab
- Resource limitation – there was, there is and never will be free engineering bandwidth
- Design to cost vs. cost of design depending on market and application

## › Process complexity

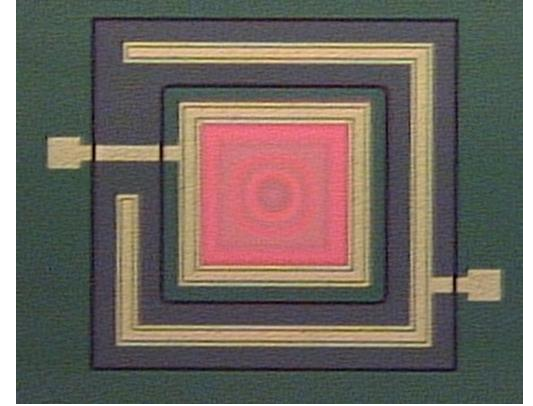
- Portfolio balancing: e.g. 1 layer vs. 3 wafer stack with 18 layers (MEMS w/o CMOS)

- No differences compared with CMOS development methodology
  - FMEA's, PCM concept, patent research, early phase reliability investigations, ....
  - Alignment with customer on development methodology
    - Frozen process spec vs. fluid spec due to concurrent process and device development
  - Sample production in non-frozen process
  
- Program management
  - Management of CMOS / MEMS interface
  - Supply chain optimization & management
  
- Problem solving methodology
  - Fishbone, 8D, 5Why, specific FA
  - Lessons learned





- Concurrent tool, process, design and packaging developments
  - Long development cycles
  - Learning cycles through supply chains are very long
- Technical differences MEMS vs. CMOS
  - MEMS control philosophy
  - CMOS equipment used for MEMS processing
    - Additional parameter control needed such as mechanical stress, topology
    - Tool operations at critical conditions – very thick process layer
    - High requirements on tolerance and homogeneities (typical tolerances for layer thickness 3%-5% MEMS vs. 10% CMOS [analog])

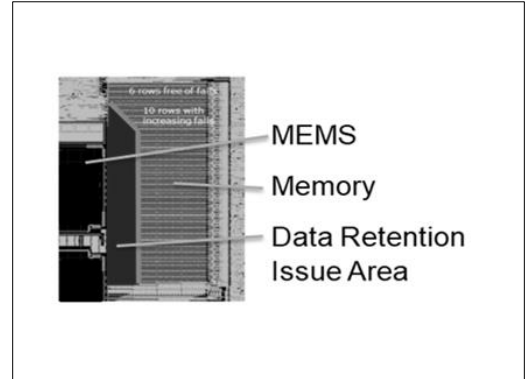
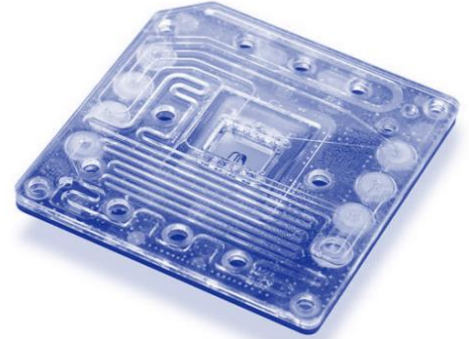


- CMOS-MEMS integration is an area of focus for X-FAB.
  - realization of very complex technologies and advanced customer products allow different ion and customer retention
  
- Opportunity to capture more value in supply chain for foundry
  - MEMS silicon value in value in final product is less compared with IC business
  
- Required technologies
  - Wafer bonding
    - Capping sensitive sensor and actuator structures
    - Manufacturing worthy integration concept, up to the assembly and packaging of the final device required
  - Through Silicon Vias
    - Manufacturing worthy integration concept, up to the assembly and packaging of the final device , required

# CMOS + MEMS WLP technology challenges



- Mechanical, electrical, chemical, physical properties have to be matched with CMOS, MEMS, Package and calibration requirements
- Fully holistic view required from project start onwards
- Examples
  1. TSV: wafer bow compensation
  2. TSV: cross contamination concerns with open passivation
  3. NVM Data retention issues caused by release etch – 100% hermetic seal required
  4. Anodic Bond for TGV: glass electrode wafer
  5. Flat passivation for bond surface preparing
  6. Fluidic optimization of polymer bond system



# WLP technology use @ X-FAB



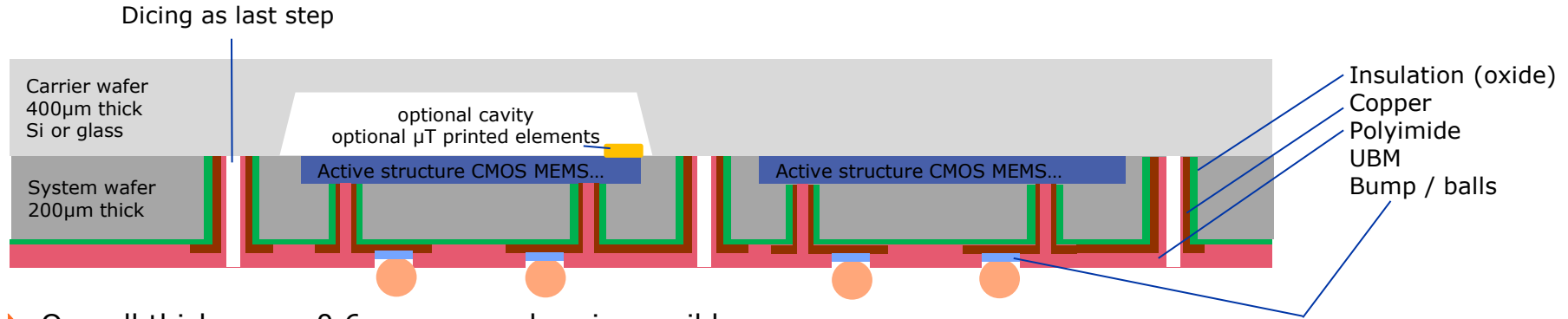
WLP	Production	Development	Comment
Anodic bonding	Pressure Sensor	Inertial Sensor $\mu$ Fluidic	High volume
Glass frit bonding	Inertial Sensor, Optical Sensor		
AlGe		Optical Sensor	
Polymer Bond	$\mu$ Fluidics		
Fusion Bond	Pressure Sensor Inertial Sensor		High volume
TSV		Optical Sensor $\mu$ Fluidic	

# X-FAB WLP Definition & Vision



## Vision

- Enable wafer level (sensor) integration and packaging up to direct mounting on PCB



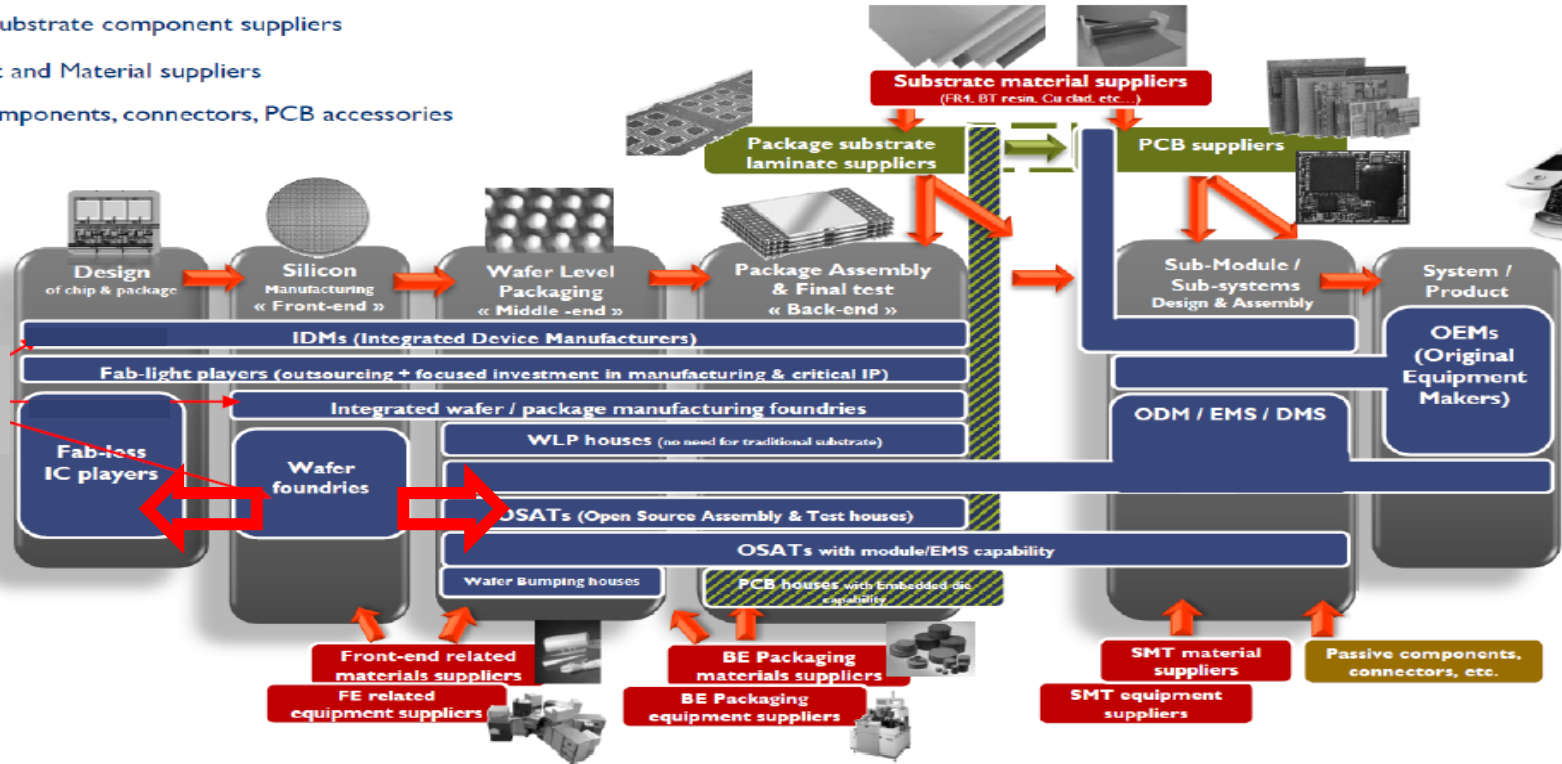
- Overall thickness – 0.6mm – even less is possible
- ALGe or Glass flip Bonding with hermetic sealing
- Grinding of system wafer after bonding – no thin wafer handling needed
- X-FAB TSV process
- Device sidewall passivation (Oxide Cu Polyimide) for all around protection of active structures
- Dicing only through the carrier wafer at end of process

# Semiconductor Supply Chain 2020 (Yole view)

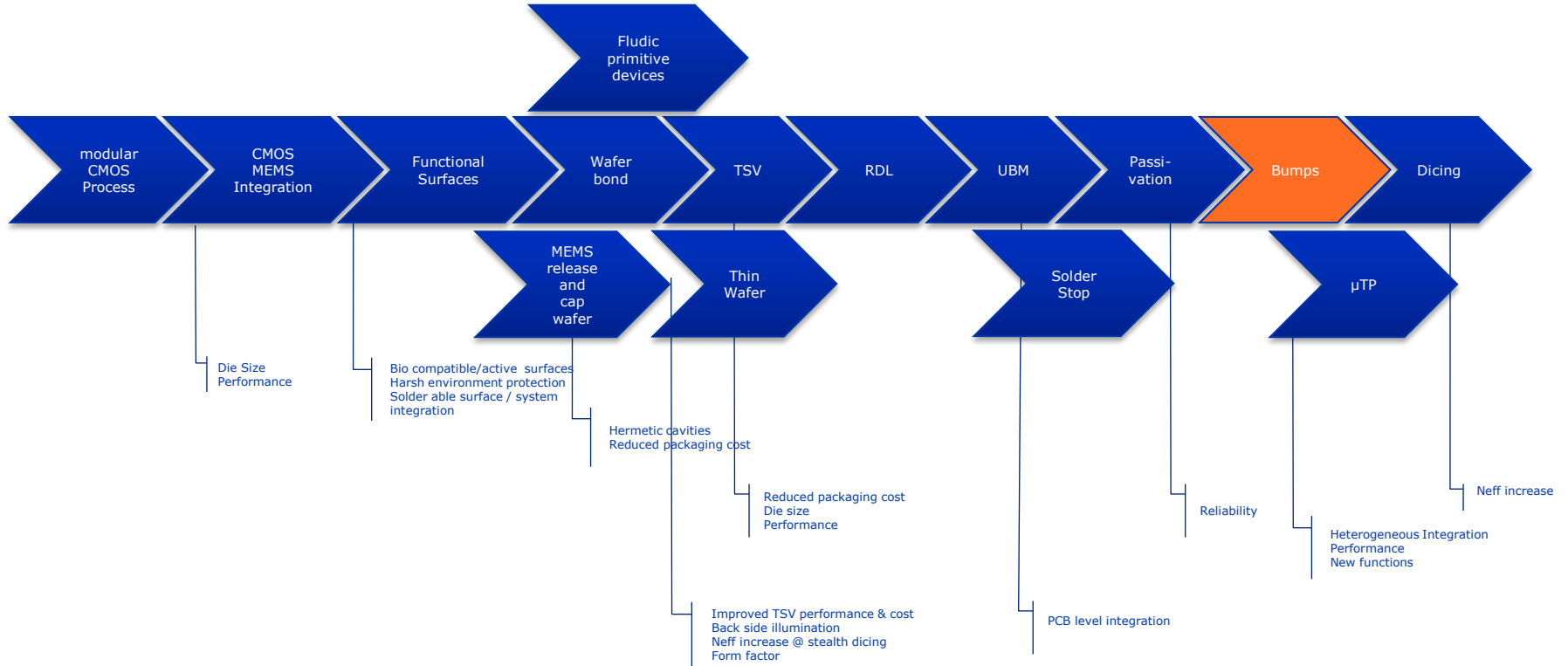


- Semiconductor production chain
- PCB and substrate component suppliers
- Equipment and Material suppliers
- Passive components, connectors, PCB accessories

X-FAB? ➔



# WLP Modular Process Concept



# Trade Off's



## > Performance

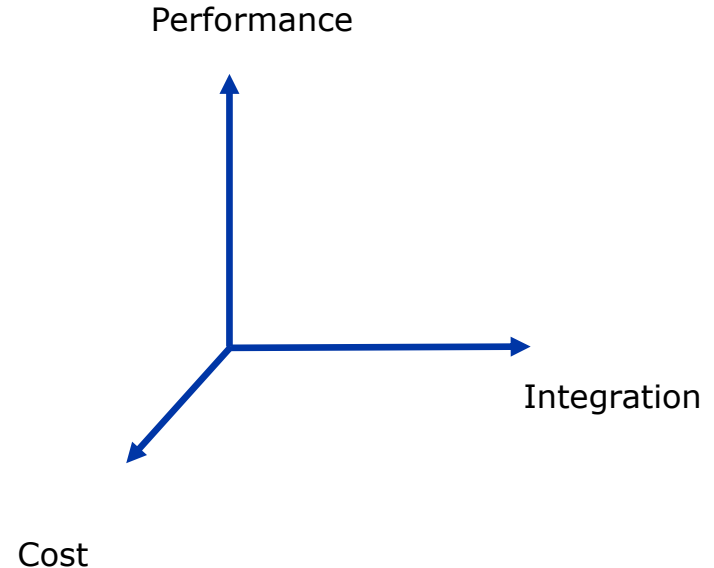
- Hermetic seal, yield, Bond Strength, Drift, reliability

## > Process Integration

- Wafer bow, release etch, open passivation , pad quality , NVM integration, temperature budget, out gassing, alignment tolerances, wafer thickness, bond frames, noble metal

## > Cost

- Process complexity
- Capex
  - Tools
  - Metrology, Monitoring
  - Cross contamination
- Opex





- Leverage of high volume mfg. experience:
  - Bond pad protection schemes in MEMS processing
    - Dicing over pads
  - Outgassing in cavities
  - Front side protection vs. edge grip handling capabilities
  - ....
- Requirements:
  - Standard Process Blocks and process module reuse
  - Gap development vs. full flow development

**Anisotropic Silicon Wet Etching**

**Process Module**

**Description**

**Characteristics and Functional Elements**

The KEM etch of silicon is characterized by a significant anisotropy of the etch rate, i.e. a direction dependence in the crystal lattice. For the relative etch rates of KEM in the main crystallographic directions it holds:

$k_{110} : k_{100} : k_{111} = 1 : 100 : 2000$

Consequently not only the mask shape but also the crystal/wafer orientation determine available structures created by KEM etching; typically arbitrary shapes cannot be created. Available structures for the most common <100> wafer orientation are shown.

X.FAB provides special customer support for the KEM etch mask design (see service offer).

**Key Features**

**Application Concrete**

- Pressure sensors
- Cap order
- Microfluidic

**Process Flow for <100> Wafer Orientation**

Step	Process	Substrate
1.	Hardmask Deposition	Substrat
2.	Photo Process (Photo-/Resistcoating alignment optional)	Substrat
3.	Hardmask Etching	Substrat
4.	Resist Removal	Substrat
5.	KEM Etching	Substrat
6.	(Optional) Remove Hardmask	Substrat

**Process Chemical**

Potassium Hydroxide (KOH)

**Final structures for Cap etching**

# Cross Contamination

- Leverage of CMOS high volume manufacturing infrastructure requires managing the risks involved
  - Objective is zero risk for CMOS WIP
- Methodology requirements
  - Developing and sustaining of specific mindset
  - Controlled material flow and related logistics
  - Additional in line tests - MEMS and CMOS specific (detailed GOX monitoring)
- Tools and infrastructure
  - Separation by clean room, main frame or chamber required
  - Dedicated tools and handling systems (supported by tool automation)





# Key Messages



- We do not expect MEMS WLP high volume manufacturing to become a commodity in the next years
- We believe managing the business model risk (large capex, small projects) is key
- We see specs for tools and process constantly being pushed to the limits and above
- We experience complex supply chain issues
- We recognize standardization and process module re-use is key

The background of the slide is a 3D rendering of a globe where the continents are composed of numerous small, blue, rectangular microchips. The globe is set against a blurred background of a sunset or sunrise sky with warm orange and red tones. A small orange and yellow light streak is visible on the right side of the globe.

# THE MORE THAN MOORE FOUNDRY.

Thank you for your attention.